

Title: A step-by-step Guide to SystemVerilog Interfaces

Presenters: CVC (Contemporary Verification Consultants Private Limited)
Srinivasan Venkataramanan (Srini), Chief Technology Officer

Presenters: Aldec®
Jaroslaw (Jerry) Kaczynski, Technical Marketing Engineer

Abstract: Modern digital designs have to transfer large amount of data across various blocks/IPs especially in the SoC arena. So traditional solutions using scalar or vector variables are too simplistic and do not allow efficient managing of data. Also they can't enforce directionality among vector fields, can't capture transfer protocol restrictions, compliance metrics etc. Fortunately, SystemVerilog introduced new construct called 'interface' that wraps data structures, transfer directions, protocol monitors in terms of assertions, cover properties and also compliance metrics via covergroups. The SystemVerilog interface also supports methods of processing the data for TLM style modeling, bandwidth measurement etc. all into one, convenient, new design entity. SystemVerilog interfaces quickly found way into new designs, as they are useful for both RTL designers and Verification engineers. This webinar explains typical elements of SystemVerilog interfaces and introduces basic concepts of using them in your designs and testbenches.

Agenda:

- Introduction
- Deficiencies of Traditional Variables
- Simple Interfaces
- Modports
- Assertions inside interfaces
- Capturing compliance metrics within interfaces
- Virtual Interfaces
- Typical Applications of Interfaces
- Are Interfaces Synthesizable?
- Conclusion and Q&A

Date/Time: 3 Live Broadcasts

South-ASIA Session

Date: 1/28/2010

Time: 12:00 pm – 1:00 pm CST- China Standard Time

([PSTBeijing](#) (China)Thursday, January 28, 2010 at 12:00:00 NoonUTC+8 hours, [Las Vegas](#) (U.S.A. - Nevada)Wednesday, **January 27, 2010** at 8:00:00 PMUTC-8 hours [New Delhi](#) (India - Delhi)Thursday, January 28, 2010 at 9:30:00 AMUTC+5:30 hours Corresponding UTC (GMT)Thursday, January 28, 2010 at 04:00:00)
9:30am Thursday 1/28 Bangalore
8pm Wed. 1/27 Nevada

EUROPE Session:

Date: 1/28/2010

3:00 pm -4:00 pm CET

([Paris](#) (France)Thursday, January 28, 2010 at 3:00:00 PMUTC+1 hour [CET](#) Corresponding UTC (GMT)Thursday, January 28, 2010 at 14:00:00 [Las Vegas](#) (U.S.A. - Nevada)Thursday, January 28, 2010 at 6:00:00 AMUTC-8 hours [New Delhi](#) (India - Delhi)Thursday, January 28, 2010 at 7:30:00 PMUTC+5:30 hours [PST](#))

7:30pm Thursday 1/28 Bangalore
6am Thursday, . 1/28 Nevada

USA Session:

Date: 1/28/2010

9:00 am-10:00 am PST USA

([Las Vegas](#) (U.S.A. - Nevada)Thursday, January 28, 2010 at 9:00:00 AMUTC-8 hours [PSTNew Delhi](#) (India - Delhi)Thursday, January 28, 2010 at 10:30:00 PMUTC+5:30 hours. Corresponding UTC (GMT) Thursday, January 28, 2010 at 17:00:00)

10:30 pm Thursday, January 28, 2010 Bangalore
9am Thursday, . 1/28 Nevada