



CVC Pvt. Ltd.

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Do-it Right - Verification using SystemVerilog with VMM (DR-VMM)

What is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

What is VMM?

Verification Methodology Manual (VMM) is a framework for Verification using SystemVerilog (SV). VMM provides a mean of doing verification in a well defined and structured way. It is a culmination of well known ideas, thoughts and best practices all bundled as a good text book. It is also supported by a standard set of base classes to help building structured verification environment faster.

What's a Do-it Right course?

Do-it Right is a series of methodology trainings from CVC for those who are familiar with the basics and want to do the verification the “right” way. For instance, SystemVerilog offers a wide variety of features that can be used in many contexts. VMM helps to focus on end goal of achieving structured, reusable verification using these various language features. CVC’s Do-it Right courses are intended for engineers with good verification background and familiarity with SystemVerilog as a Verification language and are looking at deploying it in their next project.

Overview

CVC’s VMM course gives you an in-depth introduction to the main enhancements that VMM offers, discussing the benefits and issues with the new features and demonstrating how design and verification is more efficient and effective when using SystemVerilog constructs. The course breaks down into two modules. Basic VMM module gets the user upto speed on VMM usage. In the advanced session, we delve into details of some of the advanced features of VMM such as various design patterns such as factory, callback etc. Towards the end of the course we touch up on other powerful VMM components such as VMM Scenario generator, broadcaster, scheduler and notification. Detailed usage of these components is dealt in a separate course on “Advanced VMM” from CVC. This training ends with a quick preview of next generation applications added on top of VMM such as Register Abstraction Layer, Scoreboard etc.

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Duration

Standard version is 2 days. We can also offer standard or customized versions of this training onsite or at the location of your choice.

Objectives

- To “Get Up To Speed” on VMM base classes and their usage
- To appreciate key concepts behind factory, callback and other design patterns as it applies to verification
- At the end of the course the attendees should be able to create a verification environment for a given DUT from scratch using VMM.

Prerequisites

Delegates must be familiar with Verification features of SystemVerilog. If you need to get started, we suggest you look at CVC’s VSV course which is a 2-day course. If you have queries on these prerequisites, please contact CVC.

Verification using VMM

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Session 1: Basic VMM

- Introduction to SystemVerilog /VMM
 - What is Verification Methodology Manual (VMM)
 - Why VMM?
- Transaction Based Verification
 - Overview
 - Is it language/tool dependent?
- Classes & OOP - Refresh
- Modeling Transactions

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- Creating Data models – transactions
- Basic messaging using *vmm_log*
- Methods
- Modeling Transactors
 - Types of transactors
 - Methods
 - Implementing a BFM using *vmm_xactor*
- Modeling Communication across transactors
 - Creating and using *vmm_channel*
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 - Test Flow segment
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 - Methods
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Session 2: Advanced VMM

- Messaging
 - Log
 - Severity Level
 - Various log macros
- Factory
 - Introduction, requirements
 - Methods
 - Using factory to change the generator output
- Callbacks

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- Introduction, requirements
- Façade class declaration
- Adding the callback hook in transactor
- Populating the callback method
- Registering callbacks
- Error Injection example
- Other powerful VMM components
 - Scenario Generator
 - Notifications in VMM
 - Broadcaster
 - Scheduler
 - Messaging - Promotion and Demotion
- VMM Applications
 - RAL
 - Scoreboard package

Trainer Profiles

Srinivasan Venkataramanan, CTO

<http://www.linkedin.com/in/svenka3>

- Over 12 years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel, Synopsys** in various capacities.
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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Ajeetha Kumari, CEO & MD

<http://www.linkedin.com/in/ajeetha>

- Has 8+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

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