



CVC Pvt. Ltd.

<http://www.cvcblr.com>

Fast-Track course on Verification Using SystemVerilog

What is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

What's a Fast-Track course?

A Fast-Track process is intended to cut short detailed explanations aimed at getting to the core of the subject ASAP. CVC's Fast-Track courses are intended for engineers with little extra time to spare, yet would like to learn the new and advanced verification techniques. In 1-day we cover the essential sub-set of SystemVerilog and enable to you develop complex testbenches using advanced techniques such as OOP, Constrained Random Verification and Coverage Driven Verification. As it is really time bound we will not delve into rationales on many aspects, instead will focus on getting you hands-on with the language. Also detailed discussion on OOP is not handled in this Fast-Track course.

Objectives

- ❖ To explore the new features of SystemVerilog for verification and demonstrate the improvements in verification environment efficiency from their use.
- ❖ To explain key features for verification, such as classes, OOP, randomization, and functional coverage and illustrate how to exploit these features for more efficient verification and testbench development.

Who should attend?

Practicing **Design and Verification engineers** with tight project schedules are ideal attendees. **DV managers** will equally find it useful as they can grasp the complexity of SV in 1-day without bothering about the nitty-gritty in great detail.

**#422, VIBHU Complex, 2nd Floor, 27th Main, Sector-I, HSR Layout,
Bangalore – 560102. Ph. No/Fax: 080-42134156, +91-9916176014
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Trainer Profiles

Srinivasan Venkataramanan, CTO

<http://www.linkedin.com/in/svenka3>

- Over 12 years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel, Synopsys** in various capacities.
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

Ajeetha Kumari, CEO & MD

<http://www.linkedin.com/in/ajeetha>

- Has 8+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

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Duration

1 day with labs. We can also offer customized versions of this training onsite or at the location of your choice.

Are there extended versions of these courses?

Of-course yes! Our flagship trainings on **Verification Using SystemVerilog** are originally designed for 3 variants:

- 10-day class with extensive labs and a complete project (suitable for students, jobseekers)
- 3-day class and
- 2-day class

So, depending on how much time you can invest, you pick the one appropriate to you. Needless to say – the more time you invest, the better you master this amazingly powerful language.

Prerequisites

Attendees must be familiar with Verilog and ideally, but not essentially, OOP. If you have queries on these prerequisites, please contact CVC.

Terms & Conditions

1. In general we require that the fee is paid in 100% **prior** to the start of the training.
2. For large corporate with more number of attendees to account for their internal process we do allow an exception to the above rule; however we charge an additional 25% of the training cost per attendee in such cases. In case the fee is paid after the training, the payment should be made within 1 week after the training is delivered. Any additional delay shall be charged at 10% every additional day.
3. Any “offer” price mentioned in the course announcement is applicable only for individual attendees and not for corporate.

Cancellation Policy

Course tuition is fully refundable up to one week before the class starts. Cancellations within a week (2-7 days) of the class start date will incur a **50%** cancellation fee. Those who cancel fewer than 2 days prior to the class will be billed for the full amount of the tuition. A no-show will be treated as cancellation and no refund shall be given. For genuine cases of absence, we can provide a training token that the trainee can avail in one of the future training classes subject to space availability.

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