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## **Verification with PSL**

### **1. What is PSL?**

The Property Specification Language (PSL) is an extension to VHDL and Verilog which allows sophisticated, multi-cycle assertions and functional checks to be embedded in HDL code. PSL allows simple HDL boolean expressions to be built into complex definitions of design behavior, which can be used for assertions, functional coverage and formal verification.

### **2. Overview**

CVC's PSL course gives you an in-depth introduction to the language, together with guidelines and methodologies to help you create, manage and debug effective assertions for complex design properties. The course is packed full of examples and case studies to demonstrate real life applications of the language. We also examine different approaches to coding assertions, including workarounds for the restricted language support of some tools.

### **3. Duration**

1 day crash course. We can also offer standard or customized versions of this workshop onsite or at the location of your choice.

### **4. Objectives**

- To explain the advantages of Assertion Based Verification (ABV) using the Property Specification Language (PSL).
- To describe in detail the boolean, temporal, verification and modeling layers of PSL and show how the layers are used to build assertions.

### **5. Prerequisites**

Delegates must be able to read, write and understand VHDL or Verilog code, and be familiar with running and debugging HDL simulations. The training assumes no prior knowledge of PSL.



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# **IEEE 1850-PSL, Property Specification Language**

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