



CVC Pvt. Ltd.

<http://www.cvcblr.com>

Verification Using SystemVerilog

What is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

Overview

CVC's *Verification Using SystemVerilog* course gives you an in-depth introduction to the main enhancements that SystemVerilog offers for testbench development, discussing the benefits and issues with the new features. It also demonstrates how verification is more efficiently and effectively done using SystemVerilog constructs. The course explores in depth verification enhancements such as object-oriented design, constraint random generation, and functional coverage.

Objectives

- ❖ To explore the new features of SystemVerilog for verification and demonstrate the improvements in verification environment efficiency from their use.
- ❖ To explain key features for verification, such as classes, OOP, randomization, and functional coverage and illustrate how to exploit these features for more efficient verification and testbench development.

Duration

Standard - 2 days with labs. We can also offer customized versions of this training onsite or at the location of your choice.

Prerequisites

Attendees must be familiar with Verilog and ideally, but not essentially, Verilog2001. No prior knowledge of SystemVerilog is required. If you have queries on these prerequisites, please contact CVC.

**#422, VIBHU Complex, 2nd Floor, 27th Main, Sector-I, HSR Layout,
Bangalore – 560102. Ph. No/Fax: 080-42134156, +91-9916176014
<http://www.cvcblr.com>, info@cvcblr.com**



CVC Pvt. Ltd.

<http://www.cvcblr.com>

Table of Contents

Session 1

- Introduction to SystemVerilog
 - ◆ Language evolution
 - ◆ SV Design
 - ◆ SV Assertions
 - ◆ SV testbench
 - ◆ DPI
 - ◆ API
- Abstract modeling constructs
 - ◆ Data types, type checking, type cast
 - ◆ Structure and union
 - ◆ Packages
 - ◆ Enhanced always, case/if... else, loop, flow
 - ◆ Operators
- Arrays and its operators
- SV scheduling semantics
- DUT description
- Interface
 - ◆ Grouping signals
 - ◆ Modport
 - ◆ Clocking block, skews
 - ◆ Tasks, functions
 - ◆ Transaction Level Modeling (TLM)
- Class
 - ◆ OOP
 - ◆ cast
 - ◆ inheritance
 - ◆ polymorphism
 - ◆ parameterization
 - ◆ new constructor
 - ◆ Automatic garbage collection
 - ◆ Virtual interface
 - ◆ task and function
 - automatic and static
 - void
 - extern
 - Argument pass by value/reference

**#422, VIBHU Complex, 2nd Floor, 27th Main, Sector-I, HSR Layout,
Bangalore – 560102. Ph. No/Fax: 080-42134156, +91-9916176014
<http://www.cvcblr.com>, info@cvcblr.com**



CVC Pvt. Ltd.

<http://www.cvcblr.com>

- Program construct
- Final block
- Enhanced Concurrency modeling
 - ◆ Threads – variants of fork .. join
 - ◆ Disable fork, terminate
- Inter process communication
 - ◆ semaphore
 - ◆ mailboxes
 - ◆ queues

Session 2

- Random vs. directed testing
- Need for random testing
 - ◆ Constraints in SVTB
 - ◆ Class constraint
 - ◆ Randomize success / fail
 - ◆ Inheritance
 - ◆ Randomize.with()
 - ◆ Distribution
 - ◆ Function calls in constraints
 - ◆ Array constraints
 - ◆ Pre / post randomize
- Functional coverage
 - ◆ Motivation
 - ◆ Introduction
 - ◆ Types of coverage
 - ◆ Functional coverage process
 - ◆ Covergroup
 - ◆ Coverpoint
 - ◆ Concept of binning
 - ◆ Cross
 - ◆ Sampling event
- DPI
 - ◆ Import
 - ◆ Export
 - ◆ Context
- DPI vs. VPI/PLI

**#422, VIBHU Complex, 2nd Floor, 27th Main, Sector-I, HSR Layout,
Bangalore – 560102. Ph. No/Fax: 080-42134156, +91-9916176014
<http://www.cvcblr.com>, info@cvcblr.com**



CVC Pvt. Ltd.

<http://www.cvcblr.com>

Trainer Profiles

Srinivasan Venkataramanan, CTO

<http://www.linkedin.com/in/svenka3>

- Over 12 years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel, Synopsys** in various capacities.
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

Ajeetha Kumari, CEO & MD

<http://www.linkedin.com/in/ajeetha>

- Has 8+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

**#422, VIBHU Complex, 2nd Floor, 27th Main, Sector-I, HSR Layout,
Bangalore – 560102. Ph. No/Fax: 080-42134156, +91-9916176014
<http://www.cvcblr.com>, info@cvcblr.com**