



# Course Profile Verification Using SystemVerilog

CVC Pvt. Ltd.

VTD Square, 2<sup>nd</sup> Floor, 183/3 Sarjapura Road, Dommasandra,  
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# Course Profile

## 1. Verification Using SystemVerilog (CVC\_VSV)

CVC's *Verification Using SystemVerilog* course gives you an in-depth introduction to the main enhancements that SystemVerilog offers for testbench development, discussing the benefits and issues with the new features. It also demonstrates how verification is more efficiently and effectively done using SystemVerilog constructs. The course explores in depth verification enhancements such as object-oriented design, constraint random generation, and functional coverage.

## 2. Class Details:

- Duration: 3-days full time (Can be extended up-to 5 days on need basis)
- Prerequisites: Design, Simulation, Synthesis and Verilog
- Enrolling for a class: Please refer to Registration section.

## 3. Trainers Profiles

### A. Srinivasan Venkataramanan, CTO

<http://www.linkedin.com/in/svenka3>

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips**, **Intel**, and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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## B. Ajeetha Kumari, CEO AND MD

<http://www.linkedin.com/in/ajeetha>

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

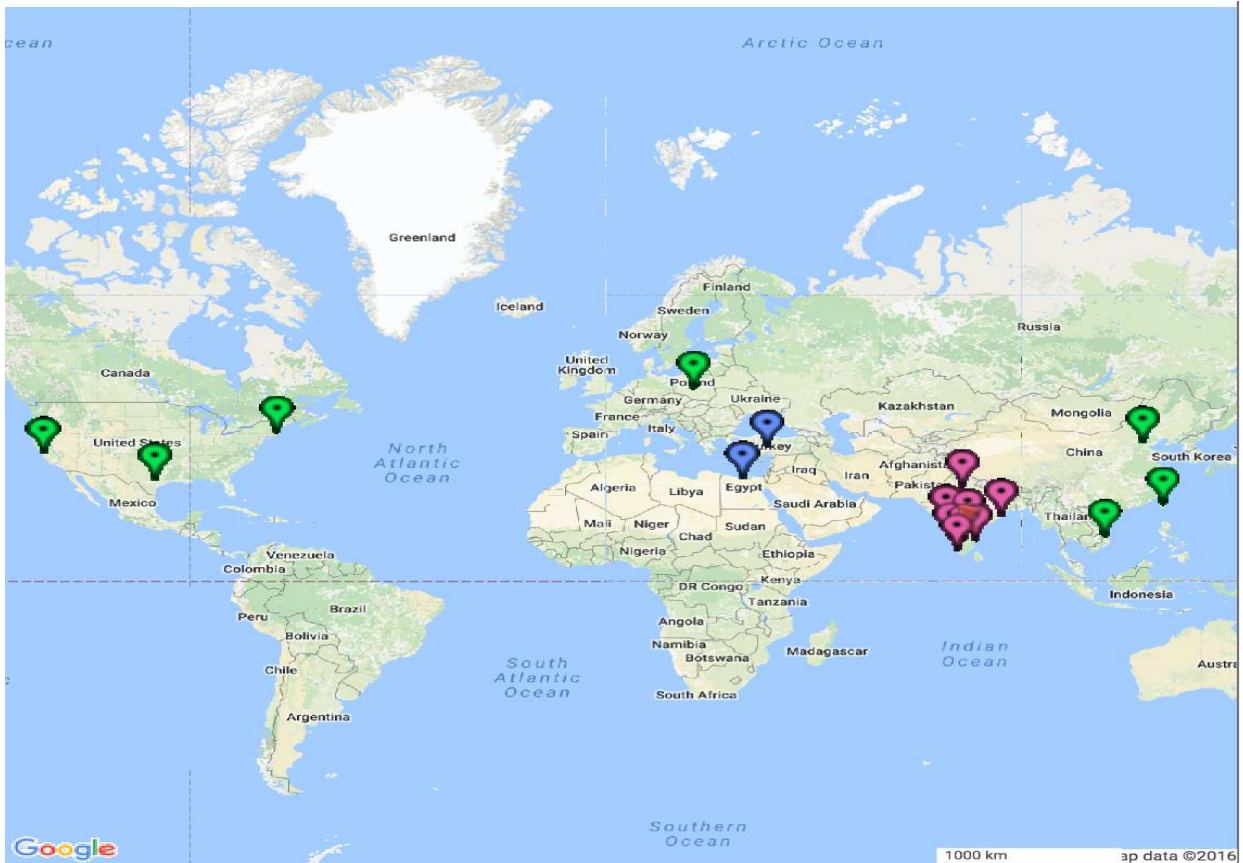
## 4. Why CVC?

Factor	Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery		World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus		Verification	Language	EDA tools
Topics covered		User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated		Last week	Months Back	As old as language was standardized
Verification Expertise		Yes	Depends on the trainer	No
Can I run labs across tools		Yes	Yes	No
Is Content Tool independent		Yes	No/Yes (Typically only one tool)	No
Global Footprint		Yes	No	Yes
Publications		Yes	No	No
Post training support		Yes	No	No
Online Technical Evaluation		Yes	No	No
Customization		Yes	No	No
Online Blogs		Yes	No	No
Extended Hands on		Yes	No	No
Code review		Yes	No	No
Architecture Review		Yes	No	No
Productivity Tools		Yes	No	No
Cost		Low	<Unknown>	Expensive

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## 5. Our Global Footprint



## 6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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## 7. Customer set (sub-set)



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## 8. Course Content

### What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented Programming features. There are also considerable improvements in the usability of Verilog for RTL design.

## Agenda

### DAY 1

#### Session 1: SV BASICS

- Introduction to SystemVerilog
  - Language evolution
  - SV Design
  - SV Assertions
  - SV testbench
  - DPI
  - API
- Abstract modeling constructs
  - Data types
    - Enums
    - Structure
  - Packages
- Arrays
  - ◆ Fixed arrays
  - ◆ Dynamic Arrays
  - ◆ Queues
  - ◆ Associative Arrays
  - ◆ Array methods
- Lab 1 – SV Basics

#### Session 2: INTERFACE

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- DUT description
  - Will use a memory controller slave model as DUT
  - Uses a proprietary “vlb” (VerifLabs Bus) interface during training
  - For AMS – will add few dummy analog/real ports with minimal logic to showcase SV features
- Interface
  - Grouping signals
  - Modport
  - Clocking block
- LAB 2 – SV Interface
  - Manual interface coding
  - Automating interface generation

### Session 3: CLASS & BFM

- Class
  - Introduction to classes
  - *new()* - constructor
  - Transaction modeling with *class*
  - Virtual interface
  - Building BFM with SystemVerilog *class*
- LAB 3 – Transactions & BFM
  - Transaction modeling
  - BFM building
  - Simple testcase using BFM

## DAY 2

### Session 4: OOP CONCEPTS

- OOP concepts
  - Encapsulation
  - Inheritance
  - Polymorphism
  - Automatic garbage collection
  - *task* and *function*
    - automatic and static
    - void
    - extern
    - Argument pass by value/reference
- Final block
- LAB 4 – Classes & OOP

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- Inheritance
- Polymorphism

## Session 5: CONCURRENCY MODELING

- Enhanced Concurrency modeling
  - Threads variants of fork .. join
  - Disable fork, terminate
- Inter process communication
  - Mailboxes
    - Standard API
    - Using it as conduit across classes/components
  - Semaphores
    - Standard API
    - Typical applications
- LAB 5 – Threads & Mailbox usage
  - Adding mailbox to Driver BFM
  - Using Mailbox to drive traffic to DUT
  - Adding a monitor component and a new free running thread
  - Adding Monitor mailbox

## Session 6: CONSTRAINT RANDOM VERIFICATION

- Random vs. directed testing
- Need for random testing
  - Constraints in SVTB
  - Class based constraints
  - Randomize success / fail
  - Inline constraints - randomize with()
  - Distribution
  - Function calls in constraints
  - Array constraints
  - Inheritance & layered constraints
- Pre / post randomize
- LAB 6 – CRV (Constrained Random Verification)
  - Adding constraints to transaction model
  - Adding a generator component (another free running thread)
  - Connect GEN – to – Driver using Mailbox

## DAY3

## Session 7: ASSERTION BASED VERIFICATION

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- Introduction to Assertions & ABV
- Structure of an assertion
- Types of assertions
  - Immediate
  - Concurrent
- Verification Directives
  - Assert
  - Assume
  - Cover
  - Bind
- Boolean layer
  - System functions
  - Sample value functions
- Sequences
  - Anatomy
  - Delay operators
  - Repetition operators
- Properties
  - Anatomy
  - Implication operators
- SV scheduling semantics
- LAB 7 – ABV (Assertion Based Verification)
  - Simple assertions, binding
  - Developing checker for given DUT using SVA

## Session 8: COVERAGE DRIVEN VERIFICATION

- Functional coverage
  - Motivation
  - Introduction
  - Types of coverage
  - Functional coverage process
  - Covergroup
  - Coverpoint
  - Concept of binning
  - Cross
  - Sampling event
- LAB 8 – CDV (Coverage Driven Verification)
  - Capturing Functional Coverage Model for the given DUT
  - Adding proper sampling
  - Run tests, collect coverage, analyze, improve

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## Session 9: DIRECT PROGRAMMING INTERFACE

- DPI
  - Import
  - Export
  - Context
- DPI vs. VPI/PLI
- LAB 9 – DPI
  - Using simple import & export
  - Integrating a C golden Reference Model to a scoreboard via DPI
  - Dynamic FCOV query API lab

## 9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to [training@cvcblr.com](mailto:training@cvcblr.com) or

Visit Us: <http://www.cvcblr.com> or

Call Us: +91-9620209223

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