Course Profile -

Assertion based verification with SystemVerilog (ABV-SVA) – basic & advanced

CVC Pvt. Ltd.

VTD Square, II-Floor, #183/3 Sarjapur Road, Dommasandra, Anekal Taluk

Bangalore – 562125. Ph. No: +91-9620209226

http://www.cvcblr.com, training@cvcblr.com

I. CONTENTS

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Course Profile

1. Assertion Based Verification with SystemVerilog (ABV - SVA)

A. What is SystemVerilog?

IEEE-1800, SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

B. What is SystemVerilog Assertion (SVA)?

SVA is an integral part of IEEE-1800 SystemVerilog languages focusing on the temporal aspects of specification, modeling and verification. SVA allows sophisticated, multi-cycle assertions and functional checks to be embedded in HDL code. SVA allows simple HDL boolean expressions to be built into complex definitions of design behavior, which can be used for assertions, functional coverage, debug and formal verification.

C. Overview

CVC's ***ABV SystemVerilog*** course gives you an in-depth introduction to the language, together with guidelines and methodologies to help you create, manage and debug effective assertions for complex design properties. The course is packed full of examples and case studies to demonstrate real life applications of the language.

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D. Objectives

- To explain the advantages of Assertion Based Verification (ABV) using the System Verilog Assertions (SVA).
- To describe in detail the boolean, temporal, verification layers of SVA and show how the layers are used to build assertions.
- To demonstrate, with examples, good and bad SVA coding styles and show workarounds for simulators with language support issues.

2. Class Details:

- Duration:
  a. 3-days for basic SVA + Q&A
  b. 3-days for Advanced SVA + Q&A
- We strongly recommend a few days break between basic & advanced sessions
- Prerequisites: Verification, SystemVerilog, basic UVM exposure
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 18+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading

books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

Ajeetha Kumari, CEO & MD

http://www.linkedin.com/in/ajeetha

- Has 17+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor \ Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint

- Headquartered in Bangalore, India
- India
  - Bangalore, Manipal, Cochin, Chennai
  - Pune, Hyderabad
  - Mumbai, Noida
- USA
  - San Jose/Santa Clara
  - Boston
  - Austin
- Europe
  - Poland
  - Munich (partner)
- Asia-Pac
  - Vietnam
  - Singapore
  - China
  - Taiwan
- Middle East
  - Turkey (partner, in the near future)

6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer list (sub-set)

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8. Course Content

What is SystemVerilog?

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What is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

Agenda

I. Introduction

- Introduction to Assertions & ABV
- Introduction to SystemVerilog
- Structure of an assertion
- Justify the use of assertions
- Why SVA and its Advantages
- Recap on UVM
- Simple UVM via Go2UVM package

II. Layers

- Types of assertions
  - Immediate
  - Concurrent
- Boolean Expression
  - Sequence
  - Disable_iff
  - Allowed data types
  - restrictions
- Verification Directives
  - Assert
  - Assume
  - Cover
  - Expect
- Clock

III. Sequences

- Declaration/structure
- Arguments
- Operations

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- Delay
- And
- Intersect
- Or
- First_match
- Throughout
- Within
- Repetition
    - Consecutive
        - *n
        - *n:m
        - *0:m
        - *n:$
    - Non-consecutive
    - Go to

IV. Properties

- Declaration/Structure
- Arguments
- Termination
- Operators
    - Not
    - Or
    - And
    - Overlapped Implication
    - Non overlapped Implication
    - If .. else

V. Linking SVA To Design (RTL)

- Bind
- In-line usage with pragmas

- Using pre-processor directives

VI. Advanced Topics

- System functions
- Recursive properties
- Assertion Overlapping
- Multiple threads
- Sequence methods
  - Ended
  - Triggered/matched

VII. Clock

- Clock resolution
- Clocking block usage
- Multi clock
  - Sequences
  - Properties

VIII. Assertion Plan

- Assertion Plan
- Assertion Plan as part of verification test plan
- Stand-alone CIP (Checker IP) plan
- Testing assertions – plan
  - Assertion testing - framework based on Go2UVM
  - Using Log predictor to make assertion tests self-checking

IX. Scheduling Semantics

- Understanding SV scheduler (Stratified event scheduling)
- Various event regions as related to Assertions
- $sampled value function usage in action blocks

X. SVA Debug

- Tunneling SVA messages through UVM messaging
- Controlling the Severity of Assertions
- Handling Assertions during Reset
- Turn OFF after first failure

XI. Common SVA Use Cases

- Standard Assertions checks
- Assertions to verify DUT clock cycle accurate behaviors
- Assertions for UVM RAL models for post-reset checks

XII. Coding Guidelines

- Good coding guidelines
- Best practices
- CIP development guidelines
- SVA Recommendation for System Level Verification
    - Selective ON/OFF
    - Assertions in post-process mode

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

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Call Us: +91- 9620209226, +91-9620209223

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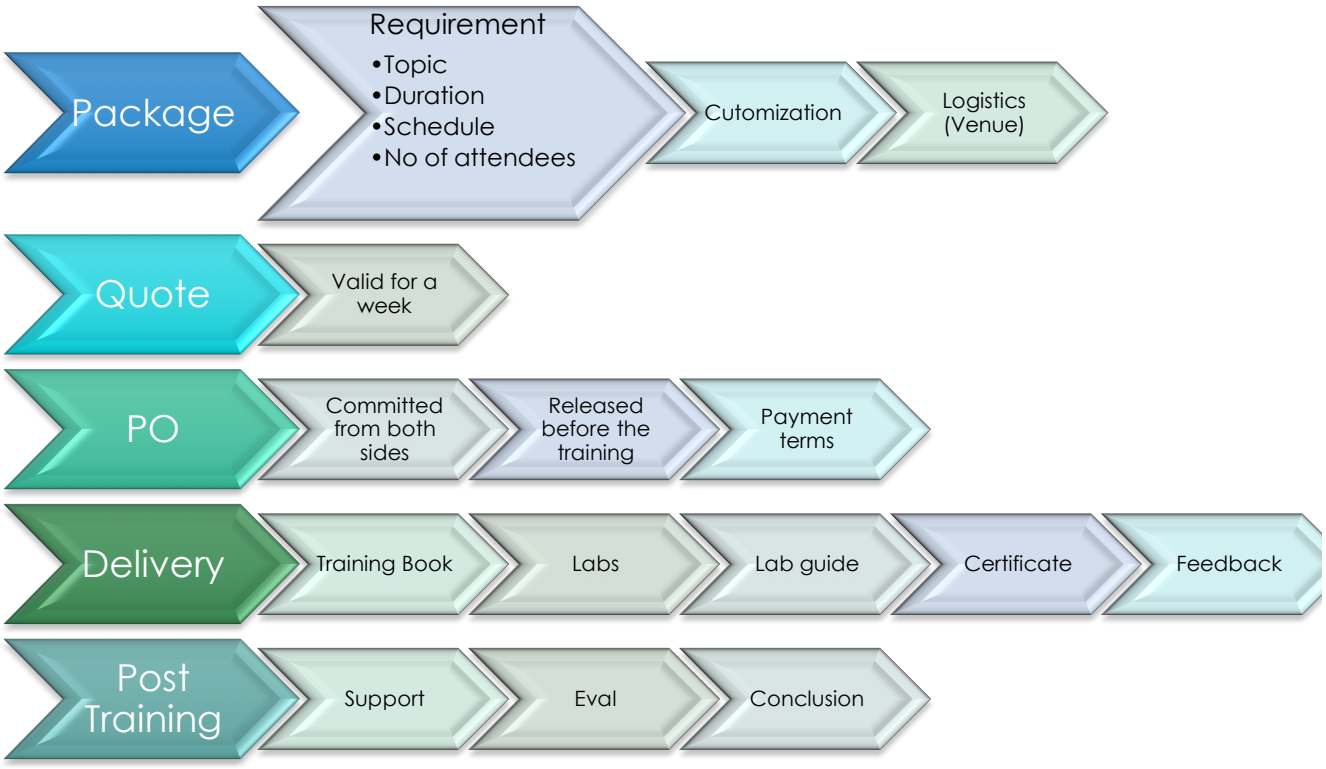
10. Engagement Process



11. More Questions?

Please contact us via email/phone: training@cvcblr.com Call Us: +91- 9620209226, +91-9620209223

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