Course Profile

SystemVerilog Assertions

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
Bangalore – 562125. Ph. No. +91-9620209226
http://www.cvcblr.com, info@cvcblr.com

I. CONTENTS

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Course Profile

1. Assertion Based Verification – SystemVerilog Assertions (ABV-SVA)

CVC's ***ABV SystemVerilog*** course gives you an in-depth introduction to the language, together with guidelines and methodologies to help you create, manage and debug effective assertions for complex design properties. The course is packed full of examples and case studies to demonstrate real life applications of the language.

2. Class Details:

- Duration: 2-days full time
- Prerequisites: Design, Simulation, Synthesis and Verilog
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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B. Ajeetha Kumari, CEO AND MD

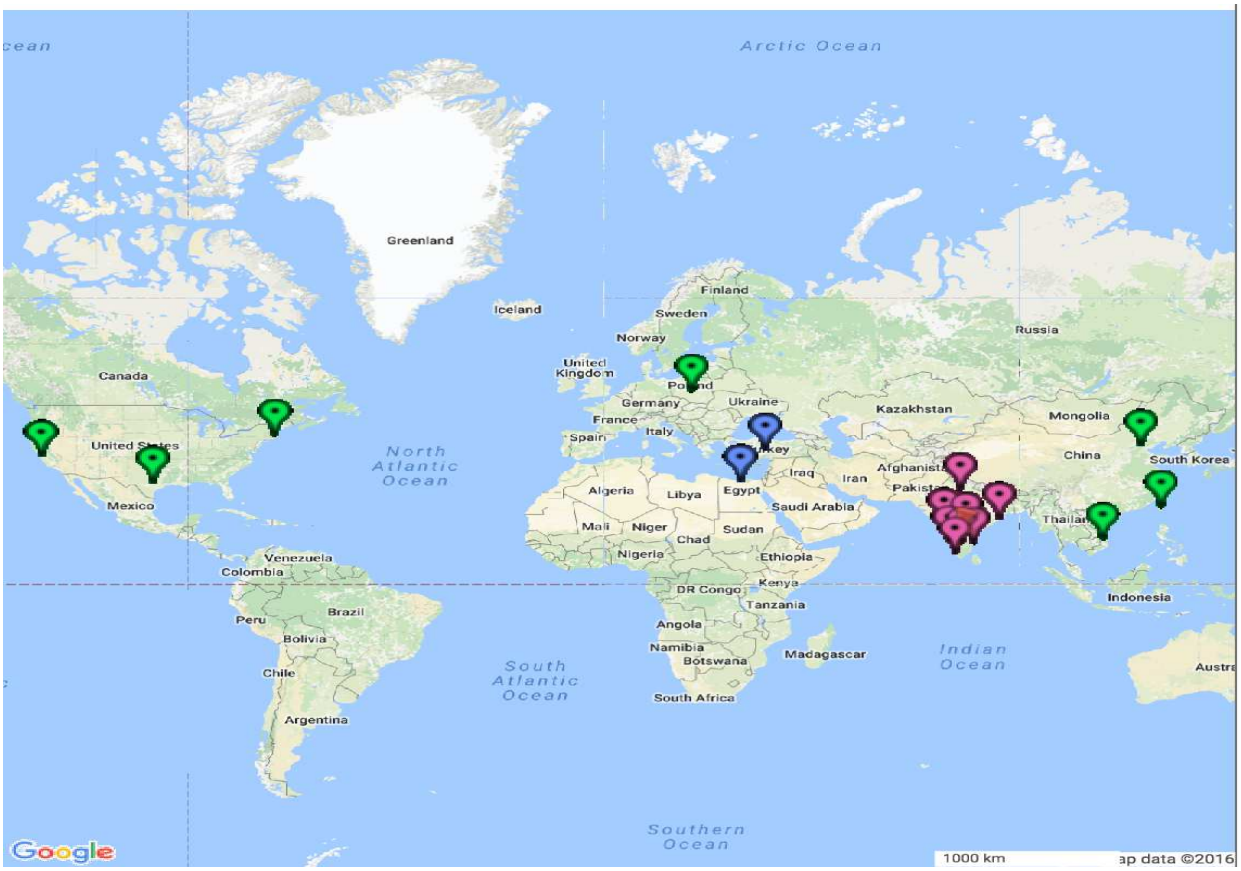
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented Programming features. There are also considerable improvements in the usability of Verilog for RTL design.

What Is SystemVerilog Assertion (SVA)?

SVA is an integral part of IEEE-1800 SystemVerilog languages focusing on the temporal aspects of specification, modeling and verification. SVA allows sophisticated, multi-cycle assertions and functional checks to be embedded in HDL code. SVA allows simple HDL Boolean expressions to be built into complex definitions of design behavior, which can be used for assertions, functional coverage, debug and formal verification.

Agenda

DAY1

Session 1: INTRODUCTION

- Introduction to Assertions & ABV
- Introduction to SystemVerilog
- Structure of an assertion
- LAB 1

Session 2: LAYERS

- Types of assertions
  - Immediate
  - Concurrent
- Boolean Expression
  - Sequence
  - Disable_iff
  - Allowed data types

- restrictions
- Verification Directives
  - Assert
  - Assume
  - Cover
  - Expect
- Clock
- LAB 2

Session 3: SEQUENCES

- Declaration/structure
- Arguments
- Operations
  - Delay
  - And
  - Intersect
  - Or
  - First_match
  - Throughout
  - Within
  - Repetition
    - Consecutive
      - *n
      - *n:m
      - *0:m
      - *n:$
    - Non-consecutive
    - Go to
- LAB 3

DAY2

Session 4: PROPERTIES

- Declaration/Structure
- Arguments
- Termination
- Operators
  - Not
  - Or

- And
- Overlapped Implication
- Non overlapped Implication
- If .. else

- LAB 4

Session 5: ADVANCED TOPICS

- Sample value functions
- System functions
- Recursive properties
- Assertion Overlapping
- Multiple threads
- Sequence methods
  - Ended
  - Triggered
  - matched
- LAB 5

Session 6: USE MODELS, GUIDELINES AND COMMON ERRORS

- Bind
- Labels
- LAB 6

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223

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