COURSE PROFILE

LOWPOWERVERIFICTION USING UPF

SITUTELAGE PVT LTD.,
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I. CONTENTS

Course Profile

1. Low Power Verification Using UPF (CVC_UPF)

Low power design of Integrated circuits is the most critical aspect of today's chip design. As the number of portable consumer electronics products increased exponentially the power consumption and battery life of the product has become the most influential selling factor. As a result many new low power design techniques has been invented and used widely. But the current hardware description languages didn't aid the designer to specify the power intent of the design. Even if it is made to support it requires rework on the existing designs and prevents code reuse. Hence a new language is required which would convey the designer's power intent to the tools. Unified Power Format which is also called in short UPF solved the problem.

2. Class Details:

- Duration: 1-day full time
- Prerequisites: Using the EDA Simulator to simulate and debug digital designs & Basics of low-power CMOS design
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

B. Ajeetha Kumari, CEO AND MD

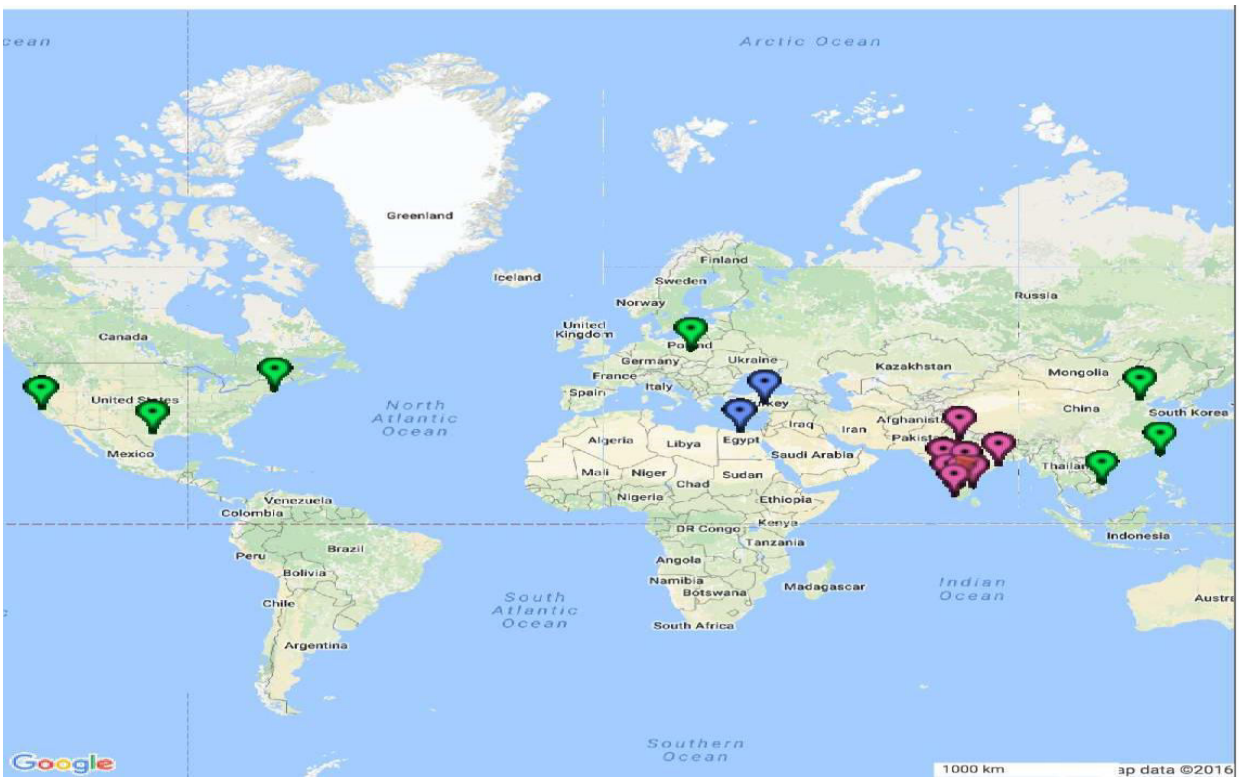
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

7. Customer set (sub-set)

8. Course Content

Low power design of Integrated circuits is the most critical aspect of today's chip design. As the number of portable consumer electronics products increased exponentially the power consumption and battery life of the product has become the most influential selling factor. As a result many new low power design techniques has been invented and used widely. But the current hardware description languages didn't aid the designer to specify the power intent of the design. Even if it is made to support it requires rework on the existing designs and prevents code reuse. Hence a new language is required which would convey the designer's power intent to the tools. Unified Power Format which is also called in short UPF solved the problem.

Agenda

DAY1

Session 1:

- About This Course
- Introduction to Low Power (LP) Design
- Introduction to Low-Power Simulation
- LAB 1
- Introduction to IEEE 1801 Unified Power Format
    - Power Domains
    - Power Network description
    - Power switches, supplies etc
- LAB 2
- Power Intent and UPF
    - Isolation
    - Level shifters
    - Retention
- LAB 3

Session 2:

- Adding Power States
- LAB 4
- Generating first-cut UPF file with DVC_LP tool

- Lab 5

- Power-Aware Simulation Coverage
- LAB 6
- UPF 1.0 -> 2.0 -> 2.1 -> 3.0 updates

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223