Course Profile

Art of debugging with UVM

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
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I. CONTENTS

Course Profile

1. Art of debugging with UVM

Given the major adoption of UVM across the globe and across the industry, advanced users are looking for tips and tricks to improve their productivity. While UVM does define a structured framework for building complex testbenches, given the strong OOP nature of UVM (and underlying SystemVerilog) and the relatively less familiar audience (as many Design-Verification, DV engineers come from hardware, electronics background and not a heavy Software background), it gets tricky for users to debug UVM based testbenches when things do not work as expected. CVC's "Art of Debugging with UVM" course gives you hands-on experience with some of the typical UVM debugging scenarios. Split into compile and run-time the course covers the breadth and depth of UVM use cases so that attendees are guaranteed to become more productive with UVM at the end of the course.

2. Class Details:

- Duration: 1-day full time
- Prerequisites: Hands-On UVM, Verification, SystemVerilog
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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B. Ajeetha Kumari, CEO AND MD

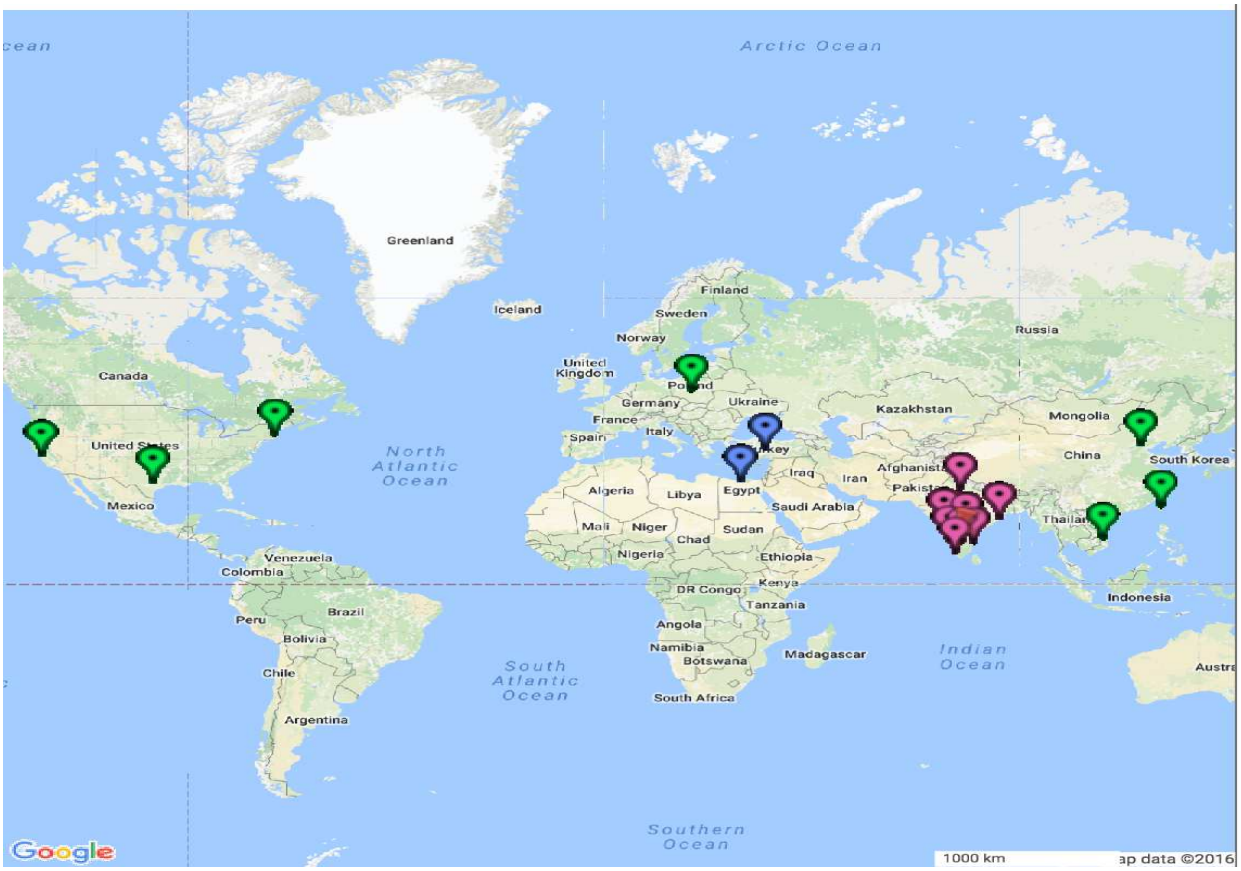
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM RAL
- UVM Level 1
- UVM Level 2
- UVM Level 3
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

Why is UVM debug challenging?

During our various training and consulting engagements using UVM we have seen DV engineers struggling to debug relatively simple UVM issues. At times the error messages are cryptic and do not point to the actual source code, rather somewhere from the base classes, making the debug difficult. This is a side effect of effective structuring of code across base classes within UVM. We have captured a series of such common issues and error messages into a collateral form that we call it as "UVM Vault".

Agenda

Session 1: Typical UVC Structure in UVM

- Introduction to SystemVerilog /UVM
  - What is Universal Verification Methodology? (UVM)
  - Why UVM?
- Quick UVM re-cap
  - Messaging, Transaction Models
  - Interface, Driver, Sequencer
  - Agent, Env, Test
- LAB 1 – AHB basic UVC

Session 2: Basic, built-in Debug Features in UVM

- Understanding UVM log files
  - Interpret print_topology
  - Report summary
  - ID based counts
- Value of UVM Field macros in debug
  - Filed macros in Components
  - Field macros in sequences
- Controlling UVM logger
  - Customizing output format
  - ID based logging
  - Command line control of UVM Log actions
  - Turning off messages selectively
- Transaction recording features
  - Classes in waveforms

Session 3: Debugging UVM Factory

- Factory Debug
  - Wrong ordering of override vs. create()
  - Overriding in run time phases
  - Factory audits
  - Debug by type
  - Instance specific override debug
  - Impact of ***name*** in instance based overrides
  - Factory ***undo***
  - Multiple overrides – replace
  - Multiple overrides - ignore

Session 4: Debugging UVM Configuration Database

- Config DB debug
  - Setters and no getters
  - Get with no set
  - Audit Config DB
  - Spell checker usage
  - UVM CLP features, interpreting the output
- Case study: Virtual interface remaining unconnected
  - Config DB set-get mismatch

Session 5: Debugging simulation hangs in UVM

- Virtual SQR debug
  - Agent being passive vs. active
  - Grab/Ungrab issues
- Objection debug
  - Phase skip debug
  - Using UVM CLP for objection debug
  - Custom end-of-test debug for productivity

Session 6: Debugging common UVM errors

- Common UVM errors and solutions
  - Compile
  - Run time

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223

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