Course Profile

UVM-Level 3

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
Bangalore – 562125. Ph. No. +91-9620209226
http://www.cvcblr.com, info@cvcblr.com

I. CONTENTS

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1. Universal Verification Methodology (UVM) – Level 3

CVC's Level2 UVM course addresses advanced topics on UVM. Attendees are expected to be fully conversant with Basic UVM and can build IP level testbenches with UVM framework. We strongly recommend attendees to self-attest/self-evaluate via online UVM quiz at www.verifjobs.com before to ensure their UVM awareness is robust to handle advanced topics in Level2 course. This Level-3 course, does quick recap of Basic UVM course, and then moves on to some of the advanced features of UVM.

2. Class Details:

- Duration: 3-days full time (Can be extended up-to 5 days on need basis)
- Prerequisites: Verification, SystemVerilog, UVM (Level-1, to the level of UVC building)
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

B. Ajeetha Kumari, CEO AND MD

http://www.linkedin.com/in/ajeetha

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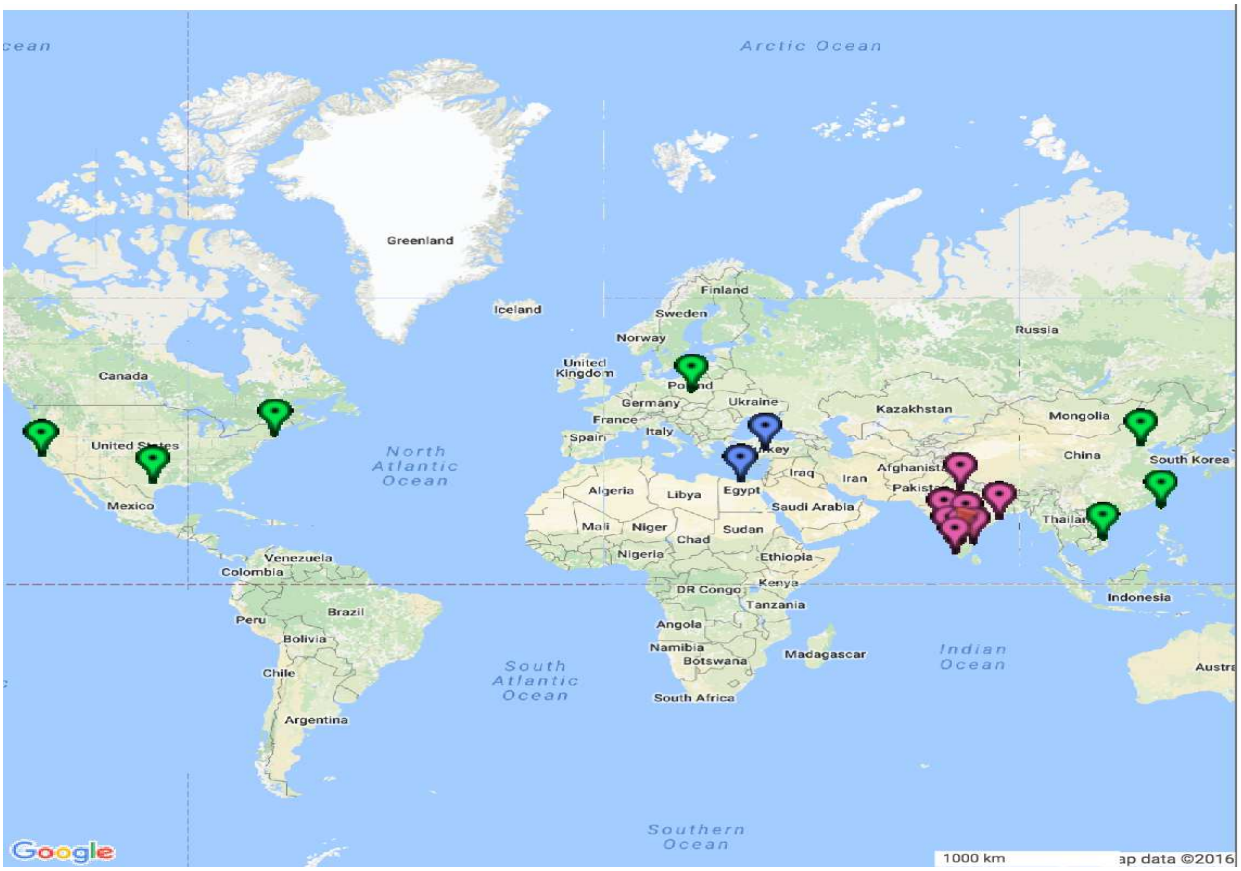
- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented Programming features. There are also considerable improvements in the usability of Verilog for RTL design.

What Is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

Agenda

DAY1

Session 1: UVM introduction, UVC building

- Introduction
- Quick UVM re-cap
  - Messaging, Transaction Models
  - Interface, Driver, Sequencer
  - Agent, Env, Test
- LAB 1 – AHB basic UVC
  - Interface, Transaction model, Driver
  - SQR, Agent, Env, simple test

Session 2: Reactive Agents

- Need for reactive agents in verification
- Reactive Slave models
    - Simple, non-pipelined
    - Pipelines slave models
    - Out of order slave models
- LAB 2 – Slave model UVC
- Interrupt controllers in UVM
    - Reactive agents
    - Reactive driver models
- Reactive sequences
    - Grab-ungrab
    - Lock-unlock
    - Debugging deadlocks (due to bad grab/lock)
- Interrupt related assertions
- Coverage model for interrupt scenarios
- LAB 3 – Interrupt UVC

Session 3: Advanced Scoreboarding Techniques

- Scoreboards, means to connect to Monitors
    - Simple analysis_imp/export
    - Multiple analysis_imp via uvm_analysis_imp_decl macro
    - Using TLM Analysis FIFO
- Out of order Scoreboard model
- Built-in UVM components for scoreboards
    - In order comparator
    - Algorithmic comparator
- LAB 4 – AHB UVC
    - Scoreboard with TLM connections to monitor

Session 4: DPI & Assertions in UVM

- Using DPI & Assertions along with scoreboards
    - Adding SVA inside interface
    - Using bind
    - Using uvm_error in action blocks
    - Using DPI to integrate C golden reference model
- Lab4 – Using assertions with UVM

- Add CIP (Checker IP) to AHB-Lite
- LAB 5 – Scoreboard with DPI
  - Golden Ref model via DPI
  - RGB--2--YUV design

Session 5: Low Power Verification in UVM

- UPF basics
- Assertions for low power
- Coverage models for state-tables
- UVM phasing for low power
  - Domains
  - Sync/Async domains
  - Sync/Async various phases
- Low Power sequences
  - Lock/Unlock
  - Seq library usage to intermix LP sequences

Session 6: RAL Models

- RAL basics
- Various access modes
- Adaptor
- Predictor → Monitor integration
- Offset porting from IP to system level
- Multiple maps
- Volatile register handling
- Safety registers
  - Modeling via callbacks
- Backdoor access
- Built-in Register sequences
- Case study – Re-partitioning for better reuse with UVM RAL

Session 7: Managing end-of-test in UVM using Objection mechanism

- Need for Objection mechanism
- Mechanics of UVM phasing leading to mandatory objection usage in UVM
- Best practices in objection usage
- Performance Issues with UVM objections

- Active components objection
- Passive components objection
- Debugging objection related issues

Session 8: Coding Guidelines

- Good coding guidelines
- Best practices

Session 9: UVM 1.2 updates

- Important changes in UVM 1.2
- Migration approach from UVM 1.1 to UVM 1.2
- Preview of IEEE P1800.2 UVM changes (from UVM 1.2)

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223

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