Course Profile

UVM-Level 1

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
Bangalore – 562125. Ph. No. +91-9620209226
http://www.cvcblr.com, info@cvcblr.com

I. CONTENTS

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Course Profile

1. Universal Verification Methodology (UVM) – Level 1

CVC's UVM course gives you an in-depth introduction to the main enhancements that UVM offers, discussing the benefits, new features and demonstrating how design and verification is more efficient and effective when using SystemVerilog constructs. Basic UVM training gets the user up-to speed on UVM usage with which one can start building IP level testbenches with UVM framework. Towards the end of Basic UVM course we touch upon some of the advanced features of UVM such as Virtual Sequencer, TLM port in-depth etc. Detailed usage of these components is dealt in a separate course on "UVM Level 2 and Level 3" from CVC.

2. Class Details:

- Duration: 3-days full time (Can be extended up-to 5 days on need basis)
- Prerequisites: Verification, SystemVerilog
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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B. Ajeetha Kumari, CEO AND MD

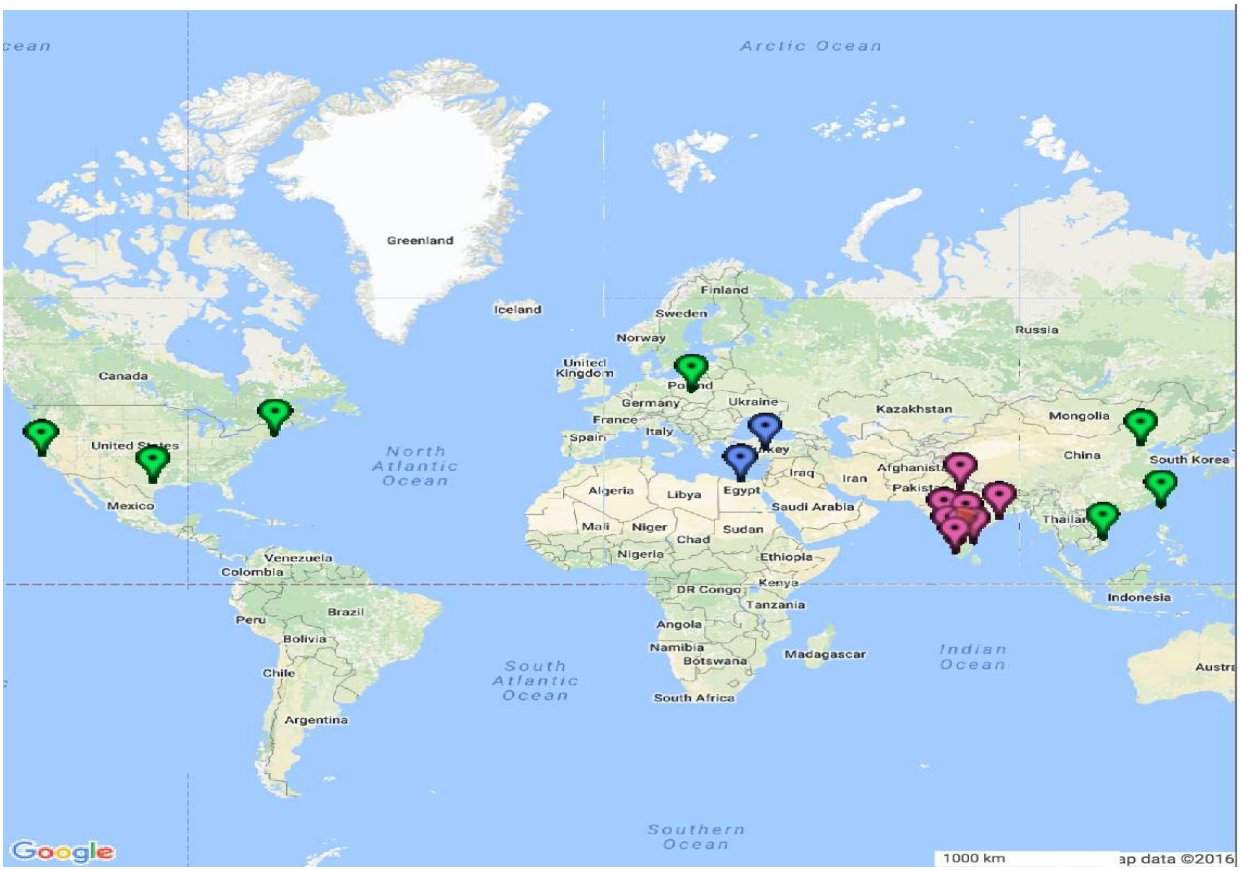
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented Programming features. There are also considerable improvements in the usability of Verilog for RTL design.

What Is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

Agenda

DAY1

Session 1:

- Introduction to SystemVerilog /UVM
  - What is Universal Verification Methodology? (UVM)
  - Why UVM?
- Transaction Based Verification
  - Overview
  - Is it language/tool dependent?
- Classes & OOP - Refresh
- DUT description
- Overall view of UVM base classes, structure (UML diagrams)
- UVM macros – need, basic usage

- Unified messaging in UVM
  - Reporting methods
  - Related macros
  - FILE & LINE number printing
  - Verbosity control from command line
- LAB 1

Session 2:

- Modeling Transactions
  - Creating Data models – transactions
  - Modeling Transactions (uvm_transaction/uvm_sequence_item)
  - Related macros
- Modeling Components/transactors
  - Types of components
  - Typical component methods (a la UVM Phases)
  - Developing Driver BFM (uvm_driver)
- LAB 2

Session 3:

- Transaction Sequencer/Generator (uvm_sequencer)
- UVM Phases
  - 1.0 phasing (OVM style)
  - 1.1 new phasing
- LAB 3

DAY2

Session 4:

- UVM agents (uvm_agent)
  - Hierarchical grouping
  - ACTIVE/PASSIVE controls
- Modeling Environment (uvm_env)
- LAB 4

Session 5:

- Creating test cases (uvm_test)
- Putting it all together

- Singleton design pattern
- uvm_top usage
- print_topology ()
- Global methods in UVM
- run_test()

- LAB 5

Session 6:

- Analysis Ports in UVM
  - Publisher-Subscriber mechanism
  - *write()* method – single subscriber usage
- Building Monitor (uvm_monitor)
- Scoreboards in UVM
  - uvm_scoreboard
  - uvm_tlm_analysis_fifo usage
- Usage of assertions as checkers
- Functional Coverage integration to UVM
  - uvm_subscriber
  - uvm_tlm_analysis_imp
- Configurations in UVM
  - uvm_config_db – Set & Get
  - Applications of Config-DB
- LAB 6

DAY3

Session 7:

- Advanced stimulus generation
  - More on Sequencer
- Sequences – how to define new sequences
  - Means of choosing sequences
- LAB 7

Session 8:

- Factory pattern
  - Concept of factory

- Type based API
- Global overrides
- Instance specific overrides

- LAB 8

Session 9:

- TLM ports – theory behind TLM
  - Port, export
- Advanced Messaging features
- Summary, closing remarks
- LAB 9

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223

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